REMARKS

The Examiner has not provided an examination of claims 29 and 30 which were added in Applicants response to the Office Action of November 11, 2005. Applicants request the Examiner provide Applicants with a indication of allowability of claims 29 and 30.

The Examiner has indicated that claims 12-24 are allowed. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

In view of the Examiner's earlier restriction requirement, Applicants retain the right to present claims 25-28 in a divisional application.

The Examiner rejected claims 1 and 11 under 35 U.S.C. §102(e) as being unpatentable over Shinogi et al. (US/6,534,387).

The Examiner rejected claims 2 and 4-9 under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. in view of Bhattacharya et al. (US/4,434,434).

The Examiner rejected claim 10 under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. in view of Miyamoto et al. (US/6,342,434).

The Examiner rejected claim 3 under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. over Bhattacharya et al. (US/4,434,434) as applied to claim 2 and in further view of Desai et al. (US/5,159,535).

Applicants respectfully traverse the §102(e) rejection with the following arguments.

35 USC § 102

As to claim 1, the Examiner states that "Shinogi et al. disclose a method of forming a semiconductor interconnect comprising a first step of providing a semiconductor wafer (20) (see Fig. 8A); as second step of forming bonding pads (8) (see Fig. 8B) in a terminal wiring level on the front side of the wafer (20); a third step of reducing the thickness of the wafer prior to any dicing operation of [on] the semiconductor wafer (see Figs. 8C and 9A); a fourth step of forming solder bumps (12) (see Fig. 9B) on the bonding pads (8); and a fifth step of dicing the wafer into bumped semiconductor chips (see Fig. 9C)."

Applicants contend that claim 1, as amended, is not anticipated by Shinogi et al. because Shinogi et al. does not teach each and every feature of claim 1. For example, Shinogi et al. does not teach "reducing the thickness of said wafer prior to initiating separation of said semiconductor wafer into individual semiconductor chips."

Applicants respectfully point out that Shinogi et al. specifically teaches in col. 2, lines 56-63 and in FIGs. 8A through 8C that "As seen from FIG. 8A, after metal posts (8) are formed on wafer (20), *grooves* (21) *are formed* by a first dicing step. Next, as seen from FIG. 8B, the entire surface of the wafer is resin-sealed by a resin layer R. Further, as seen from FIG. 8C, the wafer is divided into *individual* chips (20A) by polishing the rear surface of the wafer to *reach the bottom of each of the grooves* (21) (In this case, the individual chips(20a) are integrated by the resin R."

Applicants further point out that Shinogi et al. specifically teaches in col. 2, line 66 to col. 3 line 1 and FIGs 9A through 9C that "Thereafter, the portion of the resin layer R between the adjacent chips 20A is diced so that the wafer is separated into individual chips 20A."

Clearly, Shinogi et al. is reducing the thickness of substrate 21 *after* initiating separation of wafer 21 into individual semiconductor chips (see FIGs. 8A and 8B) not *before* as the Applicants claim 1 requires since without formation of grooves 21 in a non-thinned substrate no

individual chips 20A could be illustrated as existing in FIGs. 8C , 9A and 9B of Shinogi et al. Since claims 1-11 and 29-30 depend from claim 1, Applicants respectfully maintain that claims 1-11 and 29-30 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Gardecki et al.

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